ADCLDR PAGE 1

1 ;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

2 ;

3 ; Author : ADI - Apps www.analog.com/MicroConverter

4 ;

5 ; Date : April 2002

6 ;

7 ; File : ADCldr.asm

8 ;

9 ; Hardware : ADuC814

10 ;

11 ; Description : Performs repeated single ADC conversions on ADC0

12 ; Adjusts output of DAC0 to vary with LDR

13 ; lnk 6 needs to be in position B

14 ; lnk 7 needs to be in position B

15 ; lnk 8 needs to be on

16 ; lnk 5 needs to be on

17 ;

18 ;\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*

19

20 $MOD814 ; Use 8052&ADuC814 predefined symbols

21

0001 22 CHAN EQU 1 ; convert this ADC input channel..

23 ; ..chan values can be 0 thru 6

24 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

25 ; BEGINNING OF CODE

---- 26 CSEG

27

0000 28 ORG 0000h

29

0000 02004B 30 JMP MAIN ; jump to main program

31 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

32 ; INTERRUPT VECTOR SPACE

33

34

35 ;====================================================================

36 ; MAIN PROGRAM

004B 37 ORG 004Bh

38

004B 39 MAIN:

40

41 ; PRECONFIGURE...

42

004B 75EF80 43 MOV ADCCON1,#080h ; power up ADC

004E 75D801 44 MOV ADCCON2,#CHAN ; select channel to convert

0051 75FD3D 45 MOV DACCON,#03DH ; Dac 0 0-5V 12bits

0054 D2AF 46 SETB EA ; enable interrupts

0056 D2AE 47 SETB EADC ; enable ADC interrupt

48

49 ; PERFORM REPEATED SINGLE CONVERSIONS...

50

0058 7401 51 AGAIN: MOV A,#01H ; Delay length

005A D2DC 52 SETB SCONV ; innitiate single ADC conversion

53 ; ADC ISR is called upon completion

005C 30DFFD 54 JNB ADCI,$

005F 85DAFA 55 MOV DAC0H,ADCDATAH

0062 85D9F9 56 MOV DAC0L,ADCDATAL

57

0065 80F1 58 JMP AGAIN

ADCLDR PAGE 2

59

60 ;\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

61 END

VERSION 1.2h ASSEMBLY COMPLETE, 0 ERRORS FOUND

ADCLDR PAGE 3

ADCCON1. . . . . . . . . . . . . D ADDR 00EFH PREDEFINED

ADCCON2. . . . . . . . . . . . . D ADDR 00D8H PREDEFINED

ADCDATAH . . . . . . . . . . . . D ADDR 00DAH PREDEFINED

ADCDATAL . . . . . . . . . . . . D ADDR 00D9H PREDEFINED

ADCI . . . . . . . . . . . . . . B ADDR 00DFH PREDEFINED

AGAIN. . . . . . . . . . . . . . C ADDR 0058H

CHAN . . . . . . . . . . . . . . NUMB 0001H

DAC0H. . . . . . . . . . . . . . D ADDR 00FAH PREDEFINED

DAC0L. . . . . . . . . . . . . . D ADDR 00F9H PREDEFINED

DACCON . . . . . . . . . . . . . D ADDR 00FDH PREDEFINED

EA . . . . . . . . . . . . . . . B ADDR 00AFH PREDEFINED

EADC . . . . . . . . . . . . . . B ADDR 00AEH PREDEFINED

MAIN . . . . . . . . . . . . . . C ADDR 004BH

SCONV. . . . . . . . . . . . . . B ADDR 00DCH PREDEFINED